UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,689	03/04/2002	Takashi Hashimoto	H-1032	2817

7590 11/26/2003

Mattingly, Stanger & Malur, P.C.
Suite 370
1800 Diagonal Road
Alexandria, VA 22314

EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,689	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003* .

2a)☐ This action is **FINAL.** 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *11-16 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10; 17 &19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *06/04/02* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II , Species 1&4(Claims 1-10&17) on August 06, 2003 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10; 17 and 19-31 are rejected under 35 U. S. C. 102(b) as being anticipated by Nakajima et al. (US 5,204,276).

Regarding claims 1+9-10+17;19-23; 26-28 and 30-31, Nakajima et al., in related text (Col. 5, Line 17- Col. 7, Line 68) and figures (Figs. 2A-2F) disclose a method for manufacturing a semiconductor device comprising the steps of:

(a) depositing a silicon nitride film 7 on a semiconductor substrate1;

(b) depositing a base electrode forming silicon film 8 of a bipolar transistor on the silicon nitride film7; introducing a first impurity of a surface portion of the base electrode forming silicon film (Col. 5, Lines 38-47);

(c) depositing a first silicon oxide film 9 on the base electrode forming silicon film 8;

(d) forming an aperture that reaches the silicon nitride film on the first silicon oxide film and the base electrode forming silicon film (Fig. 2B);

(e) forming a second silicon oxide film 10 on the side surface of the base electrode forming silicon film that is exposed from the aperture by applying oxidation treatment on the semiconductor substrate such that a thickness of the second silicon oxide film at a side surface of the base electrode forming silicon film is less than a thickness of the second silicon oxide film at an upper surface portion of the base electrode forming silicon film (Col. 5, Line 38-Col. 6, Line 8 and Fig. 2C);

(f) etching and removing the silicon nitride film in isotropic fashion so that a side surface of the silicon nitride film is recessed from a side surface of the base electrode forming silicon film in the aperture by applying wet etching treatment on the silicon nitride film(Col. 6, Lines 19-30 and Fig. 2C); and

(g) forming a base region forming epitaxial layer selectively on the semiconductor substrate that is exposed from the aperture.

Regarding claim 2, after the step (d) and before the step (e), comprising the steps of: applying wet etching on the semiconductor substrate; and removing a part of the first silicon oxide film so that a side surface of the first silicon oxide film in the aperture is recessed from a side surface of the base electrode forming silicon film in the aperture and an aperture size of the

first silicon oxide film in the aperture is made larger than an aperture size of the base electrode forming silicon film (Fig. 4C-4D)

Regarding claims 3; 24-25 and 29, comprising a step of making the thickness of the second silicon oxide film formed on a region where the first impurity is introduced thicker than that of the silicon oxide film formed on the region other than the first impurity introduced region in the base electrode forming silicon film that is exposed from the aperture during the step (e), by applying a step of introducing the first impurity into a portion of the base electrode forming silicon film on the side with which the first silicon oxide film is in contact after the step (b) and before the step (c) (Col. 5, Line 38-Col. 6, Line 8)

Regarding claim 4, comprising the step of: (h) removing the entire second silicon oxide film or the exposed portion of the first silicon oxide film so that the aperture size of the first silicon oxide film is made larger than the aperture size of the base electrode forming silicon film in the aperture after the step (g) (Fig. 4C-4D).

Regarding claim 5, comprising the steps of: after the step (h), (i) depositing a third silicon oxide film 13 on the semiconductor substrate including the internal of the aperture; (j) depositing an emitter electrode forming first silicon film on the third silicon oxide film and thereafter etching back the first silicon film; (k) etching and removing the third silicon oxide film to expose the epitaxial layer from the aperture by use of the emitter electrode forming first silicon film that has been not removed in the etching back process as a mask; (l) depositing an emitter electrode forming second silicon film on the semiconductor substrate including the internal of the aperture; and (m) patterning the emitter electrode forming second silicon film to form an emitter electrode16 (Fig. 2E-2F)

Regarding claim 6, comprising the steps of: introducing the second impurity in the second silicon film in the step (e); and diffusing the second impurity in the emitter electrode forming second silicon film into the epitaxial layer to form an emitter region on the epitaxial layer after the step (m) (Col. 6, Line 62-Col. 7, Line 7)

Regarding claim 7, comprising the steps of: removing the first silicon oxide film located near the emitter electrode so that the side surface of the first silicon oxide film is recessed from the side surface of the emitter electrode; and depositing a metal film on the semiconductor substrate including the emitter electrode and then applying heat treatment on the semiconductor substrate to thereby form a silicide layer on the portion where the metal film is in contact on the emitter electrode and semiconductor substrate (Col. 7, Lines 9-68).

Regarding claim 8, wherein the metal film is deposited by means of spattering technique (Col. 7, Lines 54-56).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DV

David Vu.